IN THE ABSTRACT:

Please amend the abstract of the disclosure as follows:

An event pipeline and vernier summing apparatus for high speed event based test system processes the event data to generate drive events and strobe events with various timings at high speed to evaluate a semiconductor device under test. The event pipeline and vernier summing apparatus is configured by an event count delay logic, a vernier data decompression logic, an event vernier summation logic, an event scaling logic, and a window strobe logic. The event pipeline and summing method and apparatus of the present invention is designed to perform high speed event timing processing with use of a pipeline structure. The window strobe logic provides a ~~unique means~~ function for detecting a window strobe request and generating a window strobe enable.

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